Remarks begin on page 22 of this paper.

An **Appendix** including annotated drawing figures is attached following page 23 of this paper.

IN THE SPECIFICATION:

Page 1, substitute paragraphs [0001] through [0004] as follows:

Field of the Invention

[0001] The present invention concerns a method for the functional verification of a software model of an integrated circuit for constituting a verification platform, and the verification platform thus created.

[0002] The invention is ~~applied~~ useful during the verification phase of the design of particular specifications of an integrated circuit that meets the needs of an industrial user, usually called an ASIC (Application Specific Integrated Circuit), and also in the checkout phase of the system constituted by the ASIC physical component and the application program executed by the ASIC physical component.

Background of the Invention

[0003] In the integrated circuit field, there are two types of circuits, the so-called conventional circuits and the so-called specific circuits, called ASICs. Manufacturers of conventional integrated circuits have standard circuit catalogs wherein the references each designate a particular standardized function. For specific applications, industrial users of integrated circuits prefer to have specific circuits developed, known as ASICs. When the term HDL or HDL-type model is used, it refers to a programming language for describing an intergrated circuit that is considered to heal the lowest level relative to C^{++} language.

[0004] The various stages in the development of ASICs are the following:

- definition of a functional specification,
- modeling (defined below) of the ASIC in an HDL-type ~~hardware~~ model description language and functional verification of the design associated with this modeling,
- technological production by the integrated circuit manufacturer, and
- hardware debugging of the circuit.

Please substitute paragraph [0007] as follows:

[0007] The HDL-type modeling of the ASIC consists in the description of Boolean logic equations that express its behavior in accordance with its specification. The HDL-type programming language used is a language dedicated to the description of the hardware objects of the integrated circuit (Hardware). It contains the primitives for describing the components with their interface signals as well as storage elements such as registers or memories.

Please substitute paragraph [0025] as follows:

Summary of the Invention

[0025] To this end, the invention concerns a method for the functional verification of a software model of an integrated circuit on demand (ASIC), in a low-level programming language (for example of the HDL type), which separately handles the generation of the model and the debugging of the functional verification tests to be applied to the model of the circuit for constituting a verification platform, comprising the following two steps:

- creation of an autonomous circuit emulator, obtained by replacing the model in a low level (HDL-type) programming language physically describing the circuit under design to be validated with a high level (for example C++) abstract description generating response data structures in accordance with the functional specification of the project as a function of the stimuli received, this mode being called the "transmission mode."

- integration of the software model in low level (HDL-type) language of the circuit resulting from the design into the verification platform, and creation of the connection of the previously validated autonomous simulation configuration, in parallel, to the interfaces of the software model of the circuit, and of the connection of an environment emulator; and

- utilization of the platform as a reference for the validation of the response data transmitted by the software model of the circuit, this mode being called the "verification mode."

Please substitute paragraphs [0050] and [0051] as follows:

Brief Description of the Drawings

[0050] The invention will be better understood with the help of the following description of an embodiment of the invention and an implementation of the method of the invention, in reference to the attached drawing, in which:

-Fig. 1 is a functional diagram representing an emulator of an ASIC integrated circuit, represented with the management of an interface in an environment emulator that can include one or several interfaces,

- Fig. 2 represents the same emulator, logically connected in parallel to the software model of the ASIC circuit to be tested, or emulator of the circuit under design in the transmission mode, represented with the management of an interface in an environment emulator that can include one or several interfaces,

- Fig. 3 is a variant of Fig. 2 applied to a model of a circuit with two nodes, and

- Fig. 4 represents the internal architecture of a verifier.

Description of the Preferred Embodiments

[0051] Before describing the invention, it is necessary, in order to make it clearly understood, to establish a certain number of definitions used below.

Please substitute paragraph [0180] as follows:

[0180] It should be clear to the reader as noted earlier herein that when the term HDL or HDL-type model is used, it refers to a programming language for describing an integrated circuit that is considered to be at the lowest level relative to the so-called high-level C^{++} language, but this should not be interpreted as a limitation, as the invention also applies to any other programming language for describing an integrated circuit, such as for example VHDL or verilog or any other.